Abstract

A mixer for mixing a digital input signal with a sampled sinusoidal signal, comprising a calculating circuit for calculating multipliers (MC) of a multiplier group (MG) which exhibits a number of dividing circuits for dividing the digital input signal applied to an input of the mixer, and a number of switchable adders/subtractors, the dividing factors of the dividing circuits being Horner coefficients of the resolved multipliers (MC) of the multiplier group (MG), the adders/subtractors being controlled in dependence on a first control bit (SUB/ADD) read out of a memory; a demultiplexer for switching through a zero value or the multiplier (MC) calculated by the calculating circuit in dependence on a second control bit (zero) read out of the memory; and comprising a sign circuit for outputting the positive or negative value switched through by the demultiplexer to an output of the mixer in dependence on a third control bit (SIGN) read out of the memory.

Figure 6